

Implementation and Integration of Switch Capacitor Filters for EEG Application

Dalchandahirwar¹, R.S.Gamad²

P.G. Student, Department of Electronics and Instrumentation Engineering, Shri.G.S.Institute of Technology and
Science, Indore, Madhyapradesh, India¹

Associate Professor, Department of Electronics and Instrumentation Engineering, Shri.G.S.Institute of Technology and
Science, Indore, Madhyapradesh, India²

ABSTRACT: this paper presents implementation of switch capacitor filter with sample and hold circuit, non-overlapping clock and a gain stage using 180 nm CMOS technology. After implementation, an integration of a Sampler circuit is done with help of Implemented basic blocks with sampling frequency of 2.0 GHz. Finally complete design of band pass filter having a band width of ≤ 13 Hz is designed which is used for EEG signals application. This band pass filter is a combination of lower cut off frequency 0.7123 Hz and higher cut off frequency of 12.895 Hz which is ideal in detecting EEG Signals (Theta, Alpha, Beta and Delta EEG wave forms). Op-amp used in these circuits having a gain of 47.779 db.

KEYWORDS: sample and hold circuit, non- Overlapping clock switch capacitor filter, Electroencephalograph, Op-amp, analog to digital converter, low pass filter, high pass filter pass and band pass filter.

I. INTRODUCTION

All circuits used in Filtering, are the ultimate quotidian of electronic and electrical signal- conditioning and processing functions. Formed for high-spirited discussions and deliberation as DAC or ADC technology solution outstretch [4, 26-32].

Active filter are generally made with the help of op-amp, resistor and capacitors, to obtained linear time invariant relation or transfer function the values of these component should be absolute. When be implement this circuitry on silicon wafer it no longer going to produce same result with these values of resisters and capacitors. Secondly it bear more space to fashion such a particular values of resistor and capacitors on CMOS chip. Third are more prone to capacitor change. VLSI circuit designer provides alternative and effective technique using switch capacitor circuits which are simulated as resistance and their time constants are controlled by ratio of switch capacitor values instead of the actual value of capacitances. Switch capacitors Filters are built with the help of switches, capacitors and op-amp [5 -7].

Bedrichhosticka's 1978 paper on a MOS switched-capacitor filter marked the beginning of the dominance of switched-capacitor techniques for integrated audio-band filtering [12]. Techniques of switch capacitor filter started in early 1970's where they were used for audio-band filtering and then for mixed signal interface. These filter work on the principle of rate of transfer of charge when switch is moving from open. Position to closed position. Basic functionality of switch capacitor circuits is shown in fig.1 this circuits is simulated as a resistor.

The simplest switched-capacitor (SC) circuit as an integrator is shown in Fig.1 [1]. Made of capacitors C_1 and C_2 with an op-amp and two transistors.

For integration and accurate voltage gain switch capacitors preferred this can be done by switching a sampled capacitor onto an op-amp with a capacitor C_2 which is connected in feedback. Czech engineer BedrichHosticka was first person who design switch capacitor filters One of the oldest of all these circuits of switch capacitor is the [1, 15].

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Website: www.ijirset.com

Vol. 6, Issue 7, July 2017

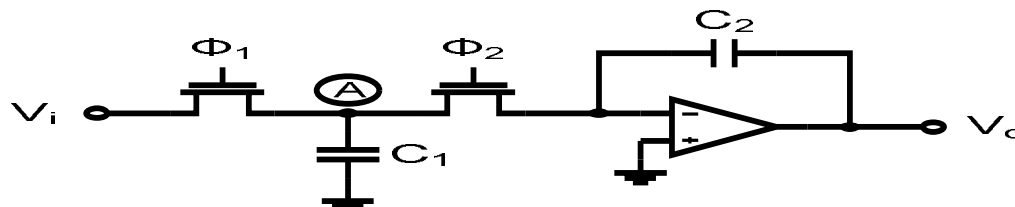


Fig. 1 switch capacitor filter as an instigator.

Parasitic-sensitive integrator develop. Analysis is shown here. Denote by $T = \frac{1}{f}$ the period of witching. In capacitors
Charge = capacitance $\times$ voltage

Then, when ϕ_1 opens and ϕ_2 closes (they are never both closed at the same time), we have the following:

C_1 has charged [17, 18]:

$$Q_1 = C_1 \times V_1 \quad (1)$$

Due to the feedback cap, C_2 , is abruptly charged with that much charge (by the op amp, which seeks a virtual short circuit between its inputs):

$$Q(t) = Q_1(t-T) + Q_2(t-T) \quad (2)$$

Equation 2 is divided) by C_2 :

$$V_2 = \frac{Q_1(t-T)}{C_2} + V_2(t-T) \quad (3)$$

And now taking invers of 1)

$$V_2 = \frac{C_1}{C_2} V_1(t-T) + V_2(t-T) \quad (4)$$

This final equation 4, shows the changes in C_2 , it increases (or decreases) its voltage with respect to each cycle corresponding to the charge that is being "pumped" from C_1 (due to the op-amp). However, there is a more fine way to formulate this fact if T is very short. Let us presents $dt \leftarrow T$ and $dV_2 \leftarrow V_2(t) - V_2(t-dt)$ and now rewrite the equation number 4, divided by dt :

$$\frac{dV_2}{dt} = f \frac{C_1}{C_2} V_1(t) \quad (5)$$

Therefore, the op-amp output equation for voltage takes the form

$$V_{out} = -V_2 = -\frac{1}{f C_1 C_2} \int V_1(t) \quad (6)$$

Where, $R = \frac{1}{f C_1}$ this permits its runtime adaptation (if we handle to make these switches oscillate corresponding to some signal given by e.g. a microprocessor)

II. RELATED WORK

In [3] this paper presents time interleaved SAH based on closed loop switch capacitor technique with different measurement results. In [4], author has come out of the basic design of integrated (ADC) analog to digital convertor which can work on input frequency of 997Hz with spurious-free dynamic range of 49.53dB. In [5], a design of a LPS and high pass filters which are suitable for detection of Electrocardiograph signals with the band of .515Hz to 150.00hz. the amplitude of such Electrocardiograph signals varies from ± 2 mv. For filtering the noise of 60Hz additional notch filter is also designed. In [6], author used the switch-capacitor filter concept for designing the high quality factor-(Q) BPF for the application of radio data system. In [7] author presented the simple design of programmable switch capacitor filter and how the high orders of such filter can be implemented suitably with in efficient area. In [8], author has presented one of the building block of switch capacitor filter e.g. two phase non-overlapping clock, it comprises of

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Website: www.ijirset.com

Vol. 6, Issue 7, July 2017

back-to-back inverters in inverted form. Popular NAND gate based without-overlapping circuit has more ingredient and more phase error involved. In [9], this paper presents analysis with design of two stage op-amp along with parameters (high gain, low power). In [10] the author has presented the design of basic circuit of switched capacitor filter on 0.35 μm CMOS technology.

III. PROPOSED ALGORITHM

Fast of all basic building block of switch capacitor filter are implemented. Then after integration done in such a fashion so that it can work as ADC.

1. IMPLEMENTATION AND INTEGRATION

A. Sample and hold circuit.

It is very simple and basic circuit it uses the MOS and load capacitor, MOS is connected in such a fashion that its gate terminal to the input continuous square wave, and drain is connected to the load capacitor to perform the function of the sampling and holding. SAH circuit is shown in fig 1. Along with NOC [15-19].

B. Non-overlapping clock.

To carry out transfer of charge through the switches, two clocks are needed but in opposite in phase. Their phase in any condition shouldn't match to run out charge lost when both switches close and open simultaneously. This is shown in fig 1. Along with SAH [20, 23].

C. Operational amplifier.

This operational amplifier uses the current mirror biasing instead of any voltage divider biasing, in order to maintain fixed current source. In addition to that, it has RC miller frequency compensation circuit a compensation circuit is necessary to sustain closed loop stability in op-amp which are operating in negative feedback [35], it is most popular to use because this can be formed by connecting a capacitor in the middle of two successive gain stages. By the effect of this capacitor an unintentional feed forward path is created thereby a right half plane zero is generated and because of this phase margin is decrease. The effect of this zero can be balanced by suitably connecting a resistor in series with the miller capacitor. It also consists of two other important architecture one is differential input amplifier stage which gives the advantage of improving overall gain and second is common source output amplifier stage provides maximum peak to peak output voltage [36-38].

INTREGATION:

In This integration part it is presented that when some of the implemented part are connected in preplanned methodology to perform the function of a Sampler. This Sampler circuit having sampling frequency of 2GHz is designed it also produces output with different phase fig. [2].

**International Journal of Innovative Research in Science,
Engineering and Technology**

(An ISO 3297: 2007 Certified Organization)

Website: www.ijirset.com

Vol. 6, Issue 7, July 2017

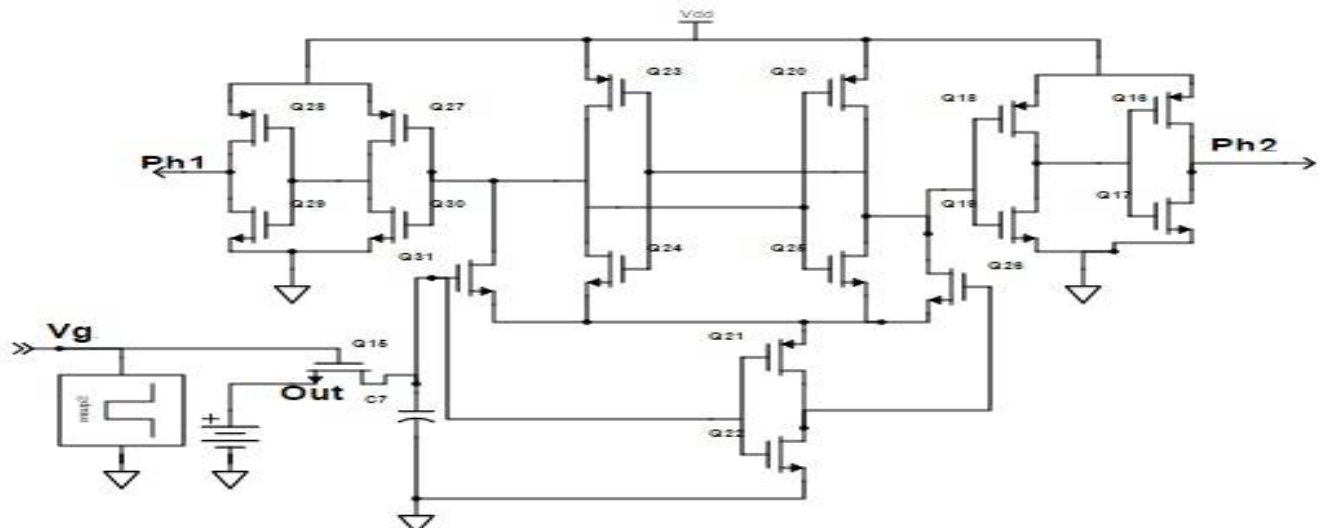


Fig. 2. ADC circuit along with its integral parts of SAH and NOC

2. BAND PASS FILTER FOR EEG APPLICATION

LPF:

This proposed circuit Fig. [3] Of low pass filter is based one of the basic topology for filter design e.i.sallen key topology. Switched capacitor circuits replace all the resistors connected in sallen key topology. This topology provides the advantage to minimizing gain bandwidth of an op-amp, this is achieved by placing op-amp just as an amplifier in this mode it is less hang on the performance of op-amp.

The desired -3db cut-off frequency for the low pass filter is 12.895 Hz. Proposed circuits has less circuit elements and low power [5].

Transfer function of low pass filter in s-domain and Z-domain is given by:

$$H_L(S) = \frac{b_0}{S^2 + a_1 S + a_0}, \text{ where } \omega_0 = \sqrt{a_0} \text{ and } H(z) = \frac{(z+1)^2}{(z - re^{-i\phi})(z - re^{-i\phi})} \text{ where } \phi = \omega t$$

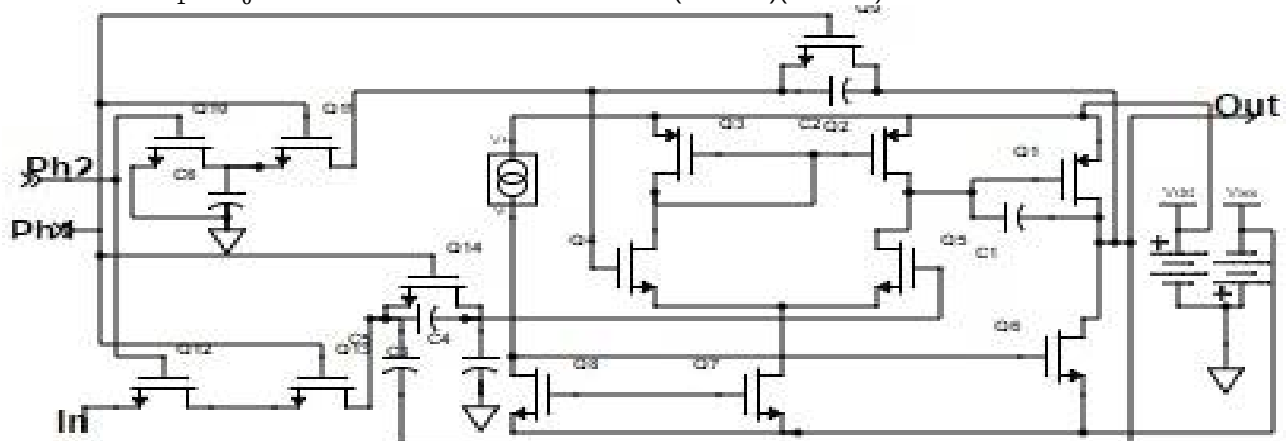


Fig. 3.circuit of second order switch capacitor LPF

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Website: www.ijirset.com

Vol. 6, Issue 7, July 2017

HPF:

This proposed high pass filter Fig. [4] Is designed using the same technique as same as low pass filter describe above. The desired -3dB cut-off frequency for the High Pass filter is 0.7123 Hz.

Transfer function of high pass filter in s-domain and in Z-domain is given by:

$$H_H(S) = \frac{b_0 \cdot S^2}{S^2 + a_1 S + a_0}, \text{ where } \omega_0 = \sqrt{a_0} \text{ and } H(z) = \frac{(z-1)^2}{z^2 - 2r(\cos\phi)z + r^2} \text{ where, } \phi = \omega t$$

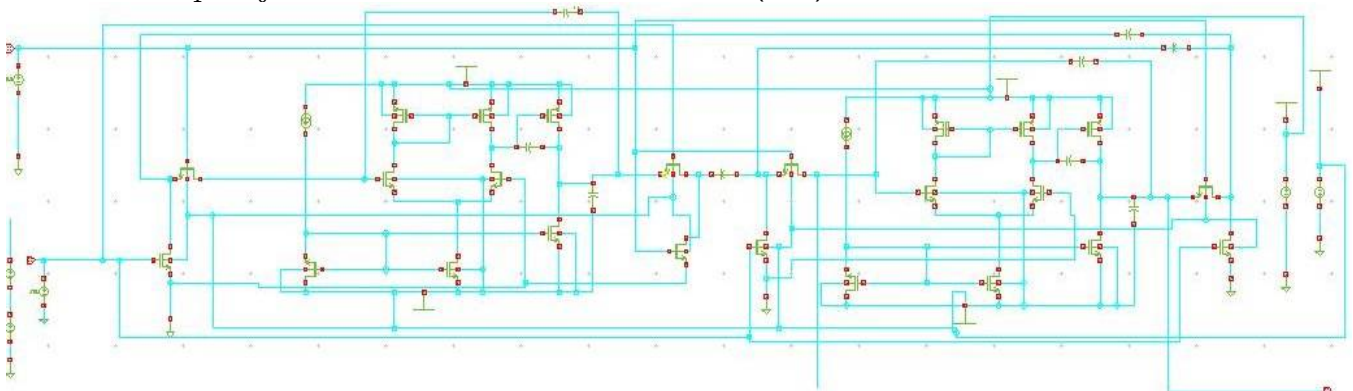


Fig. 4.circuit of second order switch capacitor HPF

BPF:

This is final proposed band pass filter Fig. [5] For EEG application having the band of less than 13Hz. Which is suitable for EEG signals.

Transfer function of band pass filter in s-domain and in Z-domain is given by:

$$H_{BP}(S) = \frac{b_0 \cdot S}{S^2 + a_1 S + a_0}, \text{ where } \omega_0 = \sqrt{a_0} \text{ and } H(z) = \frac{(z+1) \cdot (z-1)}{z^2 - 2r(\cos\phi)z + r^2} \text{ where, } \phi = \omega t$$

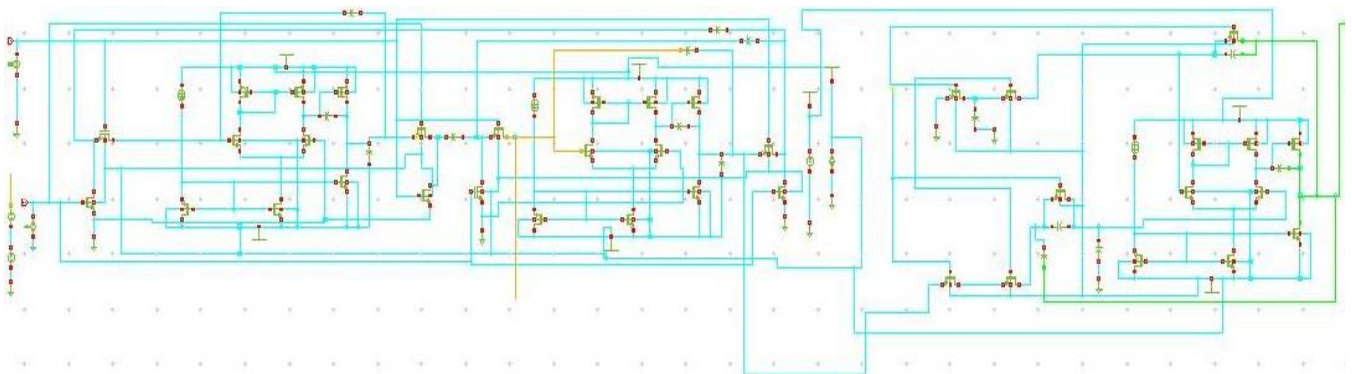


Fig. 5.circuit of second order switch capacitor BPF for EEG.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Website: www.ijirset.com

Vol. 6, Issue 7, July 2017

IV. EXPERIMENTAL RESULTS

The figure 6. Shows the out of the Sampler circuit with the total time period of 1ns which means the proper Sampling of the Continues signal the sampling frequency should be double of the time period according to the sampling theorem. The frequency response of second order low pass and high pass filter with cutoff frequency 12.895 Hz and 0.7123 Hz respectively is shown in figure 7 and 8.

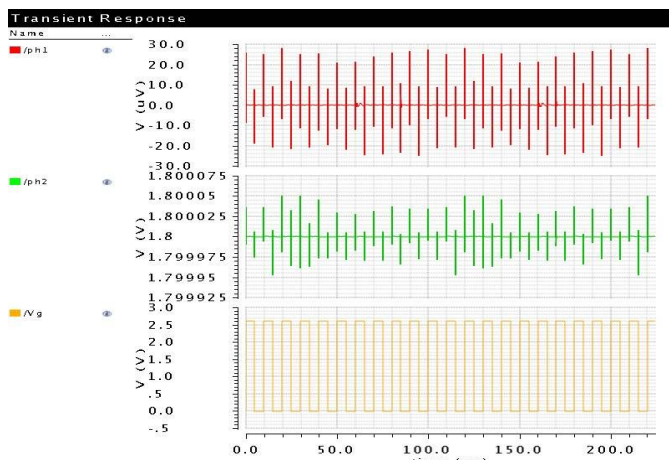


Fig. 6. The out wave form of analog to digital converter.

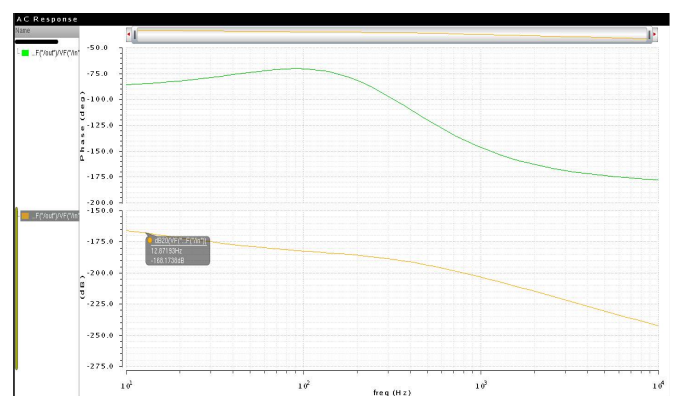


Fig. 7. Frequency response of SCF second order LPF

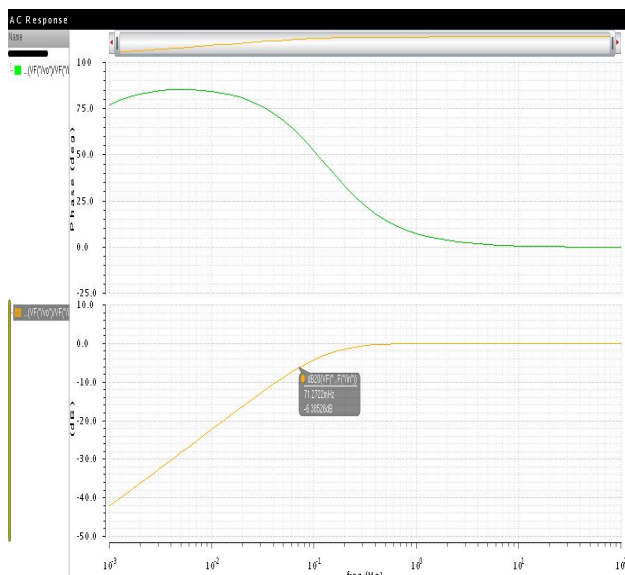


Fig. 8. Frequency response of SCF second order HPF

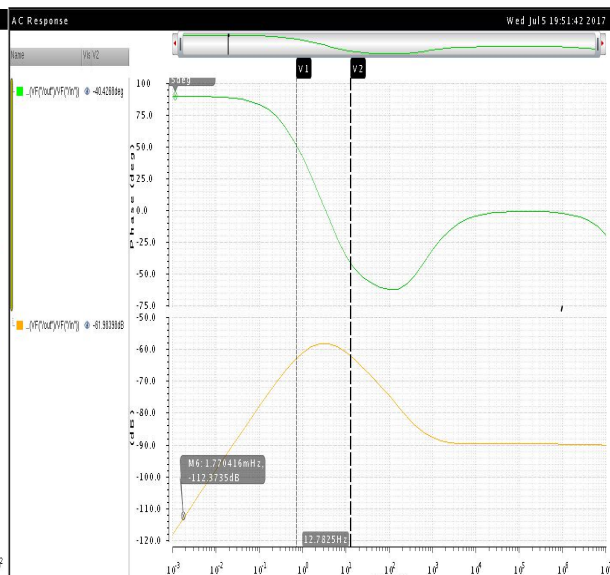


Fig. 9. Frequency response of SCF second order BPF

The final response of the EEG band pass filter is shown in figure 9.Fig.10.This Figure shows that when signal with in the band is applied to the band pass circuit, it get affected.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Website: www.ijirset.com

Vol. 6, Issue 7, July 2017



FIG. 10. FREQUENCY RESPONSE OF SCF SECOND ORDER BPF WITH INPUT EEG SIGNAL.

DESIGN PARAMETER OF PROPOSED CIRCUITS

Parameter	Performance
Supply (V _{dd})	1.8 v
DC gain (A _D) of op-amp	47.77 dB
Common mode DC gain (A _{CM})	- 26.86 dB
Bandwidth of Band pass Filter	≤13 Hz
Low pass Filter cut off frequency	12.895 Hz
High pass Filter cut off frequency	.7123 Hz
Sampling frequency of Sampler	2GHz.
Power Dissipation of LPF	195.10μw
Power Dissipation of HPF	322.13μw
Power Dissipation of BPF	579.01μw

V. CONCLUSION

To implement a fixed value of resistance its takes more space, more power and also more cost. So to replace such fixed values of resistance switch capacitor technology is used. Sampler circuit has designed with sampling frequency of 2GHz, it is useful for converting continuous analog signal to digital signal. Biomedical signals are more prone to noise, which can change many parameters of such signals e.g. EEG (electroencephalograph) signals (EEG theta, EEG alpha, EEG beta .EEG delta.) therefor band pass filter with band limit of less than 13 Hz is introduced to eliminate such noise in EEG signals.

REFERENCES

- [1] Prakruthi T.G, Siva Yellampalli,"Design and implementation of sampling and hold circuit in 180 nm CMOS Technology."International conference on Advance in computing , communication and information(ICACCI) 2015.
- [2] BjoernAlmeroth and GerhandFettweis,"Jitter requirements for band pass sampling receivers utilizing sample and hold circuit" International conference on Acoustic,speech and signal processing.IEEE 2014.
- [3] Amir Zjajo,"A1.2 V 84 db 8 mw Time –Interleaved sample and hold circuit in 90 nm CMOS technology" IEEE pp 978-1-4673-2523-3,2013.
- [4] PratapTumkur,RenuKuswamg and Darshan Shetty,"A11-bit Integration Analog to Digital Converter " Austrochip Workshop on microelectronicis,2016
- [5] Chih-Lung Hsiao, Hung-Che Wei, Ren-Bin Huang and Kuang-Ying Tan, "A Fully integrated Switched-Capacitor filter design for ECG Application," IEEE 2nd Global Conference on Consumer Electronics(GCCE), pp. 247-248, 2013
- [6] J.L.Ausin,J.F.buaque-Carrillo,G.Torelli and M.A.Domin,"A Design strategy for area effeciant High order High –Q SC Filter" IEEE,ISCAS 2004.
- [7] X.F.Wania,D.A.Johns,A.S.Sedra,"Programmable multiplexed switched capacitor filters.IEEE CH 2819-1991.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Website: www.ijirset.com

Vol. 6, Issue 7, July 2017

- [8] Ashis Kumar Mal, Rishi Todani, "Non overlapping clock (NOC) generation for low frequency switching capacitor circuits. IEEE Standard's Technology Symposium IIT Kharagpur 2011.
- [9] Mohd Haidar Hamzah, Asral Bahari Jambek and Uda Hashim, "Design and Analysis of a Two-stage CMOS Op-amp using Silterra's 0.13 μm Technology," IEEE Symposium on Computer Applications & Industrial Electronics (ISCAIE), pp. 55-59, April 7 - 8, 2014.
- [10] Meenakshi Gupta, "Design switched Capacitor filter sub circuits using 0.35 micron AMS technology," in proceeding of International Conference on Mechanical and Electronics Engineering (ICMEE), vol.1, pp.V1-6-V1-9, 1-3 Aug. 2010
- [11] P. E. Allen and D. R. Hollberg, CMOS Analog Circuit Design, Oxford University Press, 2nd edition, 2002.
- [12] Bedrich J. Hosticka, "Switched Capacitor Filters Grew the Communications Industry" A JSSC classic paper. 1978
- [13] Yang Long, Wong Zongmin, Zhou Liang and Feng Wenxiao, "A Low Power sample and hold circuit for 16 bit 100 MS/S pipelined ADC". BMTI Beijing 100076 China IEEE 2016.
- [14] Mazhar B Toyel, Ahmed Kh. Mahoud, "MEMS Switch as High Speed Sample and Hold Circuit" ISBN 978-89-968650-5-6 ICACT 2015. (WE)
- [15] Dong Li, Hong Zhang, Qing Wang, Anghao and Jun cheng, "A Negative Voltage Generator for the sample and hold circuit charge domain pipelined ADC" 978-1-4799-3282-5/14 ICISCT 2014, China, IEEE 2014.
- [16] Manal Lagziri, Fortunato C. Dualibe and Eugenio G. Moreno. "Input Switch configuration for sample and hold circuit in Low voltage operation" IEEE catalog number CFP 1454 E-CDR.
- [17] L. Zou, J. Pathrose, K. T. C. Chai, M. Je and Y. P. Xu. "Sample and hold circuit with dynamic switch leakage compensation" Electronic Letter 10 October 2013 pp. 1323-1325.
- [18] Alireza Abolhasani, Khayrollah Hadidi, Mohammed Tohidi and Abdollah Khoci. "A new high resolution and High-speed open loop CMOS sample and hold circuit" IEEE 2013.
- [19] H. C. Seol, Y. C. Kwon and O. K. Kwon "Small area low-ripple chopper instrumentation amplifier using sample and hold circuit." Electronics Letter 12 September pp 1203-1205 IEEE 2015.
- [20] Chandan Kumar, Shatrughnakumar, A. K. Mal. "An efficient two phase NOC generator for low frequency application." IEEE 2014 (ICACCCT).
- [21] D. Suvakovic, C. Salama. "Two phase non-overlapping clock Adiabatic differential cascade voltage switch logic (ADCVSL) IEEE International solid-state circuits conference. 2013
- [22] W. C. Athas, L. "J". Svensson, N. Tzartzanis. "A resonant signal driver for two phase, almost non-overlapping clock." IEEE 2016.
- [23] R. Spilka, G. Hilber, A. Rauchenberger, D. Gruber, M. Sams and T. Ostmann. "Generation of non-overlapping clock signals without using a feed back loop." IEEE 2012.
- [24] Ashis Kumar Mal, Rishi Todani. "Non-overlapping clock generation for switched capacitor circuit in bio-medical application." IEEE International conference on signal processing, communication, computing and networking Technologies (ICSCCN) 2011.
- [25] Om Prakash, Hari, Ashis Kumar Mal. "Low power and area efficient implementation of N-phase non-overlapping clock generator using GDI Technique." IEEE 2011.
- [26] Yang Xiang, Fan Xiangning, Zheng Hao. "Design of sample and hold circuit for a reconfigurable ADC." International conference on computer science and service system 2012.
- [27] Haitao Liu, Qing Deng, Hao Zhang, Shushan Xie. "Design of ADC Applied in GPS Receivers" International congress on Image and signal processing (CISP), IEEE 2017.
- [28] Alao A. Abuolsaud, Saeed Maian Qaisar, Sara H. Ba-Abdullah, Zainab M. Al-Sheikh, Mohammad Akber. "Design and Implementation of a 5-bit Flash ADC for Education" 978-1-5090-5306-3 IEEE 2016.
- [29] Shakti Prasad senapati. "Design of a simple digital ADC using only digital clocks and delay element circuit. International conference on recent trends in electronics information communication technology." May 2016 India.
- [30] Yasser S. Abdulla. "Design of a compact N-bit ADC with serial output." International conference Electrical, Electronics and Optimization Techniques (ICEEOT) 978-1-4613-9939-5 IEEE 2016.
- [31] Wei Tang, Ahmad osmani Dongsookim, Brian Goldstein, Chen Xi Huang, Vincent A. Pieribone, Eugenio Culurciello. "Continuous Time level Crossing Sampling ADC for Bio-potential." Regular papers, Vol. 60, No. 6, June 2013.
- [32] Jayamala Adsul, P. P. Vaidya and J. M. Nair "A new method of reconfigurable ADC using calibrated Programmable Slopes." V.E.S. Institute of Technology, Chembur Mumbai IEEE 2016.
- [33] Arun K. R. Riya Balwani, Priya Wagh, Prachi Salankar. "Design of op-amp using CMOS Technology and its Application." International Conference Electrical, Electronics and optimization (ICEEOT). IEEE 2016.
- [34] Frode Larsen. "Versatile Low voltage, Low power op-amp Design." AT&T Microelectronics/Bell Laboratories.
- [35] I. A. Koullias. "A wide band low -offset current-feedback op-amp Design" CH2771-4/89/0000 IEEE 1989.
- [36] J. Zhou, R. M. Ziaadeh, H.-H. Ng, H.-T. Ng, and D. D. Allstot. "Charge-pump Assisted low -power/Low -voltage CMOS op-amp Design. 0-8979-903-3/97/08 ACM. 1997.
- [37] Biplab Panda, S. K. Dosh, S. N. Mishra "High slew rate op-amp design for low power Application" International conference control, Instrumentation, communication and Computation Technologies (ICICCT) 978-1-4799-4190-2/14/IEEE 2014.
- [38] Md. Nadim Ferdous Hoque, Hasnain Ahmad, Ahmed Kamal Reza, Sharif Mohammad Mominuzzaman and A. B. M. Harun-Ur-Rashid. "Design optimization of high frequency op-amp using 32 nm. (CNFET). 6th International conference on Electrical and Computer Engineering ICECE. 2010.
- [39] Muhamed Zaidi, Ian Grout, Abu Khari A'aim. "Pole -Zero Estimation and Analysis of op-amp Design with Negative miller compensation" 6th International conference on modern circuits and system Technology (MDCAST) 2017.